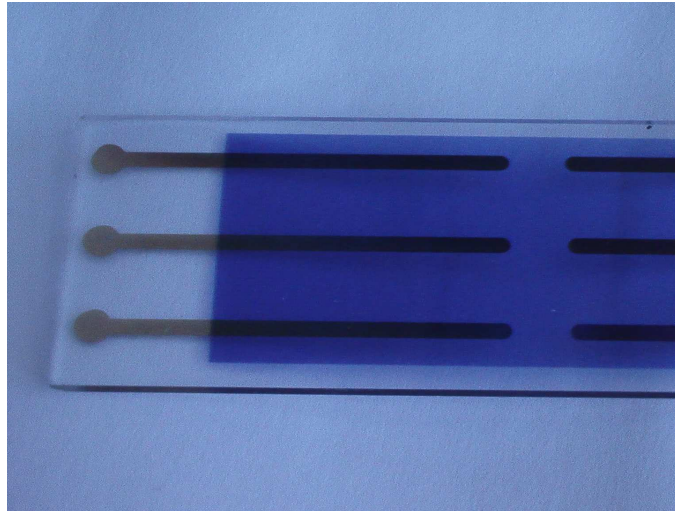


Pentacene-based organic transistors



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Abstract

This report discusses some of the electrical and optical properties of thin films of the organic semiconductor pentacene fabricated using thermal evaporation. Conductivities of between $1.84 \times 10^{-8} \Omega^{-1} \text{ cm}^{-1}$ and $7.49 \times 10^{-8} \Omega^{-1} \text{ cm}^{-1}$ are reported. Transistors using thermally evaporated pentacene were fabricated and mobilities of up to $0.03 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$ were obtained.

Contents

Contents	1
1 Introduction	2
2 Background	4
2.1 Organic (semi)conductors	4
2.1.1 Electron transport in organic materials	5
2.1.2 Pentacene	5
2.2 Transistors	6
2.2.1 Surface Treatments	7
2.2.2 Mathematical modelling	7
2.2.3 Fabrication methods	9
3 Experimental details	11
3.1 Substrates	11
3.2 Pentacene deposition	11
3.3 Conductivity experiments	11
3.4 Transistor fabrication	12
3.4.1 Alternative gates	12
4 Results and discussion	13
4.1 Pentacene spectrum	13
4.2 Conductivity	14
4.2.1 Glass conductivity	14
4.2.2 Pentacene conductivity	15
4.3 Transistors	15
4.3.1 DMDS surface treatments	16
4.3.2 A higher mobility transistor	16
4.3.3 Alternative gates	17
5 Conclusions and Further Work	22
5.1 Conclusions	22
5.2 Further Work	22
References	24
A Regression program	26

Chapter 1

Introduction

Organic transistors are currently the subject of substantial international research, with many potential commercial applications. Compared to traditional silicon devices, they have low production costs; much of the processing can be performed at or near room temperature; and the techniques involved tend to be simpler than for silicon.

Since the first postulation of organic conductors in 1911 and particularly since they were first discovered in 1954, research has progressed to the point where, today, organic devices are appearing in commercial products in increasing volume. Whilst organic transistors will never fully replace silicon due to speed issues, there is a multitude of applications, such as flexible displays, where their particular qualities far outweigh the speed benefits of silicon. Figure 1.1* shows some transistors on a flexible substrate — it is this major advantage over traditional silicon transistors that allows the fabrication of “paper” displays.



Figure 1.1: Flexible organic transistor

*Picture from
<http://www.bell-labs.com/org/physicalsciences/timeline/1998-transistor-expansion.html>

This work is concerned with the properties of thermally evaporated thin films of pentacene and pentacene-based thin film transistors. Chapter 2 gives an introduction to organic conductors and semiconductors, and to thin film transistors. Chapter 3 details the experiments performed, with the results obtained reported in chapter 4. Chapter 5 summarises the work done and makes suggestions for future work.

Chapter 2

Background

2.1 Organic (semi)conductors

Most organic materials are electrical insulators with values of electrical room temperature conductivity in the range 10^{-9} - 10^{-14} S cm $^{-1}$ [6] (10^9 - 10^{14} Ω cm resistivity). However, it was predicted in 1911 that certain organic solids may exhibit an electrical conductivity comparable to that of metals; this was later confirmed in 1954 when Akamatu *et al.* reported a room temperature conductivity of around 10^{-1} S cm $^{-1}$ for a bromine/perylene complex [1]; perylene (see figure 2.1) itself being an insulator with a room temperature conductivity of around 10^{-15} - 10^{-17} S cm $^{-1}$. Considerable further work was done in synthesising and investigating properties of both donor and acceptor molecules; a major milestone was the synthesis of the acceptor molecule tetracyano-*p*-quinodimethane (TCNQ) and the donor molecule tetrathiafulvalene (TTF), which were combined in 1972 to form the charge transfer salt (TTF)(TCNQ). This was the first organic solid to show metallic conductivity over an extended temperature range [5].

As further work was undertaken into organic metals, it was found that some TTF derivatives exhibited superconducting properties; a notable one is a charge-transfer salt of bisethylenedithiotetrathiofulvalene (BEDT-TTF, see figure 2.2), κ -(BEDT-TTF) $_2$ Cu(NCS) $_2$ (κ denoting the packing arrangement of the BEDT-TTF molecules), which has a critical temperature of 10.4 K [19, pages 76,107].

Meanwhile, in 1977, Shirakawa, MacDiarmid and Heeger (Nobel Prize in

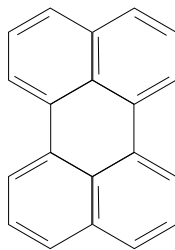


Figure 2.1: Perylene molecule

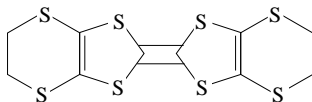
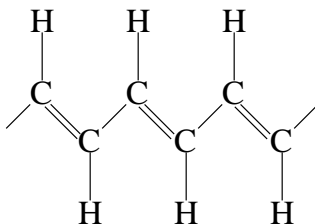


Figure 2.2: BEDT-TTF molecule

Figure 2.3: *trans*-isomer of polyacetylene

Chemistry 2000) discovered that oxidation of one of the polyacetylene film isomers (*trans*-isomer, shown in figure 2.3, is the thermodynamically stable form at room temperature [18]) with halogens made the films $\sim 10^6$ times more conductive than the unhalogenated film [18]. This paper led to a large amount of research into conducting polymers (distinct from the research into conductive low molecular weight organic materials).

2.1.1 Electron transport in organic materials

Most organic solids are insulators due to two principle reasons. First, the highest occupied molecular orbital (HOMO) of most molecules is completely filled, and there is a significant energy difference to the lowest unoccupied molecular orbital (LUMO). Secondly, the solids are usually molecular, not possessing a system of covalent bonds extending over macroscopic distances and hence quantum mechanical interactions between the HOMOs of adjacent molecules are small and the valence band formed by these interactions is very narrow. Similarly, the conduction band arising from the interactions between the LUMOs is also small, so the band gap is essentially that of the free molecule. This is also true for any σ -bonded polymers (e.g. polyethylene).

To obtain a larger conductivity and hence semiconducting behaviour, the HOMO–LUMO gap needs to be reduced; this can be achieved with extensive π -bonding, or including heteroatoms with lone pair electrons (e.g. polyacetylene, polyaniline or polyaromatics). This reduced band gap allows electrons to more easily jump between conduction and valence bands and gives rise to the semiconductive properties [5].

2.1.2 Pentacene

The experiments in this work are concerned with the organic compound pentacene (figure 2.4), a linear acene consisting of five benzene rings which acts as a *p*-type semiconductor. Linear acenes are important materials in electrical ap-

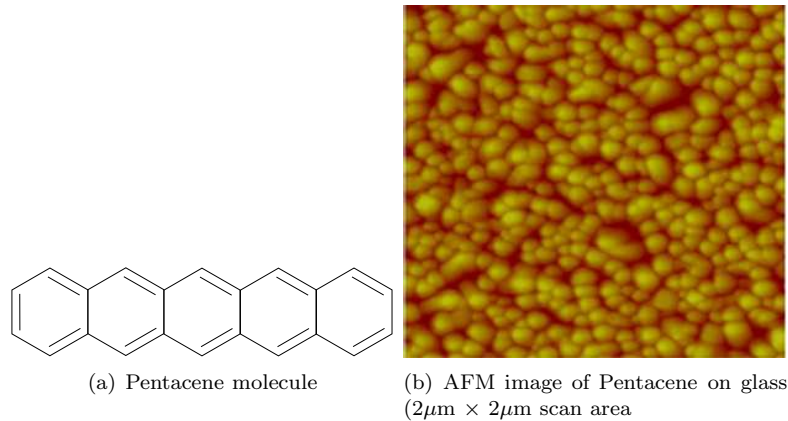


Figure 2.4: Pentacene

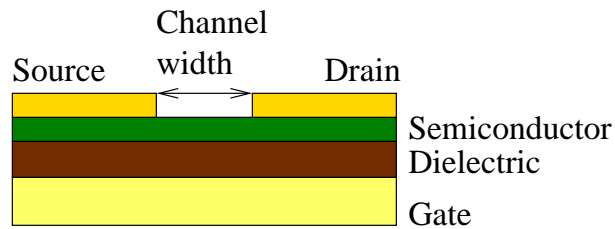


Figure 2.5: An idealised Thin Film Transistor

plications as their band gap is controllable by selecting the number of aromatic rings [14] (the more rings, the smaller the band gap).

Although most published pentacene work involves creating devices (such as transistors or diodes [9]), Minakata *et al.* have investigated doping pentacene films with iodine and alkaline metals [12, 13, 14]; achieving maximum conductivity of 150 S cm^{-1} for highly ordered films heavily doped with iodine, and 2.8 S cm^{-1} for a rubidium-doped film, which turned the film into an *n*-type semiconductor.

2.2 Transistors

The work in this report involves fabricating thin-film field effect transistors, an idealised structure of which is shown in figure 2.5.

Given that pentacene acts as a *p*-type semiconductor, the majority carriers will be holes. When a negative gate voltage is applied, an electric field is formed across the dielectric, causing an accumulation region of holes at the dielectric/semiconductor boundary. Applying a voltage to the source-drain contacts thus allows a current to flow across this accumulation layer between the contacts.

2.2.1 Surface Treatments

It is often desirable to modify the dielectric layer by application of a surface treatment — this has been shown to increase transistor mobilities. In this report, the silicon oxide dielectric is treated with a silanising solution of dimethyldichlorosilane (DMDS) in heptane. Figure 2.6 shows how the surface of the silicon oxide is modified with the DMDS solution.

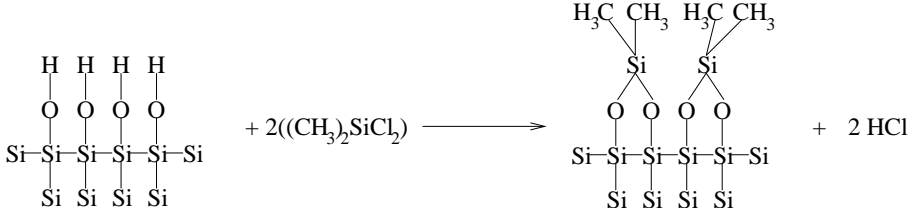


Figure 2.6: Treatment of silicon with DMDS solution

The surface of the silicon oxide has OH groups bonded to it. During silanisation, the hydrogen atoms at the surface are replaced by $(\text{CH}_3)_2\text{Si}$, which results in a hydrophobic surface. This substitution reduces the number of potential electron traps, and hence increases the mobility of the charge carriers.

2.2.2 Mathematical modelling

Consider a thin-film transistor with a channel length L and width w ; gate insulator thickness d_{OX} ; active layer material is p -type and in the on state has a p -accumulation channel with a hole mobility of μ . The simplest model (Shockley model), the (above threshold) drain current of the transistor depends on drain-source and gate-source voltages V_{DS} and V_{GS} respectively as

$$I_{\text{D}} = \begin{cases} \mu \frac{w}{L} C''_{\text{OX}} (V_{\text{GS}} - V_{\text{th}}) V_{\text{DS}} - \frac{1}{2} V_{\text{DS}}^2 & V_{\text{DS}} < V_{\text{GS}} - V_{\text{th}} \\ \mu \frac{w}{L} C''_{\text{OX}} \frac{1}{2} (V_{\text{GS}} - V_{\text{th}})^2 & V_{\text{DS}} > V_{\text{GS}} - V_{\text{th}} \end{cases} \quad (2.1)$$

Here, $C''_{\text{OX}} = \epsilon_0 \epsilon_{\text{OX}} / d_{\text{OX}}$ is the insulator capacitance per unit area at V_{th} is the threshold voltage [17].

At the saturation current (i.e. current not dependent on V_{DS}), the mobility can be obtained (graphically) by plotting the square root of the saturation current against gate voltage and obtaining the gradient; the gradient will then be

$$\text{gradient} = \sqrt{\frac{1}{2} \mu \frac{w}{L} C''_{\text{OX}}}$$

This can be rearranged to obtain a mobility

$$\mu = \frac{2 \text{gradient}^2 L}{w C''_{\text{OX}}} \quad (2.2)$$

As thermally evaporated pentacene is polycrystalline and has large grains, a grain-boundary barrier model (see figure 2.7) can be applied to understand

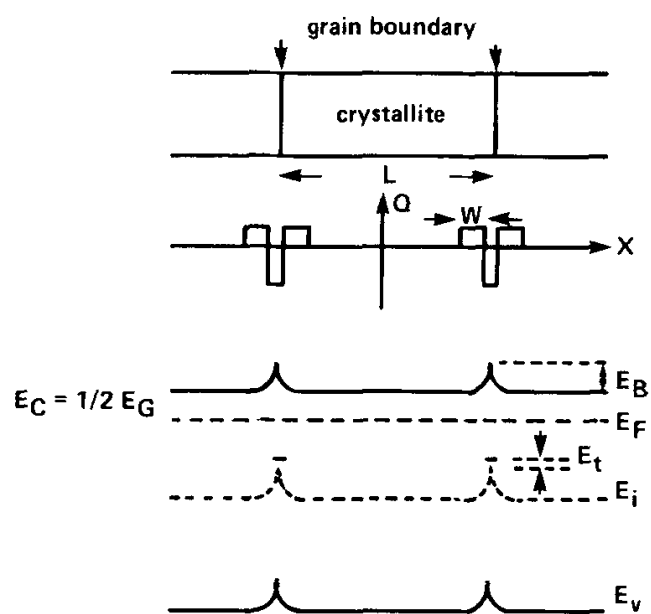


Figure 2.7: Grain structure, charge distribution and band diagram assumed in the grain boundary trapping model (taken from [10]). This diagram refers to n -type grains, not pentacene's p -type.

carrier transports. This model assumes that carriers are transported at inter-poly-grains by thermionic emission over the grain boundary barrier and that no scattering is taking place in the grains [10]. The trap density N_t can be determined from a Levinson plot of $\ln(I_D/V_G)$ against $1/V_G$. The Levinson model is based on the predicted transistor drain current in the linear regime [20], given by

$$\begin{aligned} I_D &= \mu_0 V_{DS} C_i \left(\frac{W}{L} \right) V_G \exp \left(-\frac{E_B}{kT} \right) \\ &\equiv \mu_0 V_{DS} C_i \left(\frac{W}{L} \right) V_G \left(-\frac{s}{V_G} \right) \end{aligned} \quad (2.3)$$

where E_B is the potential barrier height, μ_0 is the trap-free mobility, and the thermally activated mobility is

$$\mu = \mu_0 \exp \left(-\frac{E_B}{kT} \right) \equiv \mu_0 \exp \left(-\frac{s}{V_G} \right) \quad (2.4)$$

Screening causes E_B to fall as V_G increases, hence N_t can be estimated from the slope s of the Levinson plot using the formula

$$s = \frac{q^3 N_t^2 t}{8\epsilon k T C_i} \quad (2.5)$$

where t represents the thickness of the semiconducting layer, and ϵ is the dielectric constant of the semiconductor (which can be taken as 4 for pentacene) [20].

2.2.3 Fabrication methods

There is a large amount of published literature about pentacene transistors, discussing different fabrication methods and different substrate/gate/insulating materials. A brief summary of some reported results and materials used is tabulated in table 2.1.

Authors	Structure	Mobility
Wang <i>et al.</i> [20]	Glass substrate, sputtered Cr for gate, SiO ₂ prepared by PECVD for dielectric layer	0.43 cm ² V ⁻¹ s ⁻¹ (vacuum); 0.11 cm ² V ⁻¹ s ⁻¹ (air)
Klauk <i>et al.</i> [7]	Glass substrate, Ni gate with Pd contacts (used do to large work function improving carrier injection into the pentacene), SiO ₂ dielectric, formed by ion-beam sputtering	0.6 cm ² V ⁻¹ s ⁻¹
Qiu <i>et al.</i> [16]	Glass substrate, ITO gate, spin-coated PMMA dielectric, gold contacts	4.2×10 ⁻² cm ² V ⁻¹ s ⁻¹ (initially, reducing over time with device in air); 2.6×10 ⁻² cm ² V ⁻¹ s ⁻¹ (encapsulated in UV resin, and remaining fairly constant over time)
Daraktchiev <i>et al.</i> [3]	Si substrate, SiO ₂ dielectric activated by exposure to oxygen-plasma for 5 min in 0.1mbar O ₂ atmosphere at -40V bias	0.1 cm ² V ⁻¹ s ⁻¹
Majewski <i>et al.</i> [11]	Polyester foil substrate, titanium evaporation followed by anodisation in 10 ⁻³ M citric acid using Pt counter electrode to make TiO ₂ insulation, capped with a thin spin-coated layer of poly(α-methylstyrene)	0.8cm cm ² V ⁻¹ s ⁻¹ (threshold voltage of -0.49V)
Baude <i>et al.</i> [2]	Glass substrate, Ti/Au gate contacts, Al ₂ O ₃ dielectric formed via electron-beam evaporation, styrene-based polymeric surface treatment solution cast onto dielectric to improve transistor mobilities	1.5 cm ² V ⁻¹ s ⁻¹

Table 2.1: Mobility and structure for various transistors reported in literature

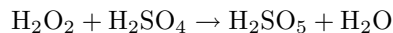
Chapter 3

Experimental details

3.1 Substrates

Glass slides were used as substrates. These were cleaned initially using acetone, placed in an ultrasonic bath for 15 minutes, followed by cleaning in peroxymono-sulphuric acid* for 30 minutes. This, being a very strong oxidising agent, is able to destroy a number of possible surface contaminants, (e.g. phenols, alcohols, aldehydes and ketones [4]).

The acid was formed by reacting hydrogen peroxide with sulphuric acid [4]



3.2 Pentacene deposition

Pentacene was deposited on the cleaned glass slides using thermal evaporation.

The material was placed in a temperature-controlled crucible in a vacuum chamber [6], which was then evacuated using a rotary pump / diffusion pump combination to a pressure of approximately 2×10^{-5} mbar. The crucible was slowly heated until the pentacene started to evaporate (with evaporation rate and film thickness being measured by an Edwards FTM5 Film Thickness Monitor). Once sufficient pentacene was deposited (approximately 90 nm, as measured by a Zygo white-light interferometer after deposition), the power to the crucible was turned off and the chamber let up to air.

An optical absorption spectrum (300 - 900nm) was recorded for the deposited pentacene, using a Perkin-Elmer UV-NIR spectrophotometer.

3.3 Conductivity experiments

Gold was evaporated through a shadow mask to form a set of equidistant contacts (1.4 mm separation) on top of the pentacene layer, which which were then used to measure the resistance of the thin film.

*Also known as Caro's acid, named for the German chemist Heinrich Caro who first prepared it in 1898

Additionally, a set of chrome-gold contacts was evaporated through an identical shadow mask onto a clean glass wafer so that a comparison could be made between the resistance of glass and that of the pentacene thin film.

3.4 Transistor fabrication

Organic thin-film transistors were fabricated, using thermally evaporated pentacene as the semiconducting layer and silicon substrates.

Highly doped n-type silicon wafers (with resistivities varying between $0.1 \Omega \text{ cm}$ and $1 \times 10^{-3} \Omega \text{ cm}$) were cleaned in the same manner as the glass slides (section 3.1), followed by etching in hydrofluoric acid to remove any oxide that may have been on the wafer. The wafer was then placed in an oxidation furnace for around 90 minutes at $1100 \text{ }^\circ\text{C}$. Ellipsometry measurements gave the thickness of the oxide at 110-130 nm, with each wafer having a variation of around 10 nm across the surface. The silicon dioxide was placed in dimethyldichlorosilane (DMDS) solution for around 5 minutes; this resulted in a hydrophobic layer on the SiO_2 (see section 2.2.1), and was used to increase transistor mobilities (see section 4.3.1).

Approximately 20-40 nm of pentacene were thermally evaporated onto the silicon oxide, followed by about 30 nm of gold to provide source and drain contacts. The gold was evaporated through a shadow mask which allowed the source/drain contacts to be patterned in a way that each transistor was isolated, and the channel width was $50 \mu\text{m}$ or $70 \mu\text{m}$, depending which mask was used.

To create the gate, some oxide was removed from the back of the wafer, silver paste applied to the exposed silicon, and aluminium foil attached to the silver paste.

Transistor characteristics were then measured using an HP picoammeter / DC Voltage source under ambient conditions (lab light and open to the atmosphere).

3.4.1 Alternative gates

As an alternative to using silver paste and Al foil on the reverse of the wafer, two methods of fabricating a gate on the top of the wafer were attempted.

S1813 photoresist was spin-coated onto the wafer, soft-baked for a minute (at $65 \text{ }^\circ\text{C}$) and a small area exposed to UV light. The exposed resist was removed by immersing in Microposit 351 developer[†]. The wafer was placed in hydrofluoric acid in order to remove the exposed SiO_2 (the photoresist was HF resistant hence the unexposed SiO_2 remained intact). Once the oxide was etched back, the remainder of the photoresist was exposed to UV light and removed in the developer.

Approximately 200 nm of aluminium was evaporated onto the exposed silicon (through a mask) and was annealed at $350 \text{ }^\circ\text{C}$ for half an hour in nitrogen. Pentacene and gold were deposited on the silicon oxide (as in section 3.4), with the aluminium being masked off. As a slight modification, instead of removing the photoresist and then evaporating aluminium onto the wafer, the aluminium was evaporated over the entire wafer including the photoresist; the resist being removed using acetone in an ultrasonic bath.

[†]This was mixed with deionised water in the ratio of 1 part developer to 4 parts H_2O

Chapter 4

Results and discussion

4.1 Pentacene spectrum

The absorption spectrum of the deposited pentacene (section 3.2) is shown in figure 4.1. As can be seen from the spectrum, there is an absorption peak in the red region of the spectrum, and the pentacene is transmissive in the blue region. This is borne out by the colour of the film, as can be seen in figure 4.2. The spectrum is comparable to one obtained by Manakata, Nogoya and Ozaki[12], with a major absorption peak at 680 nm, and a smaller one around 580 nm.

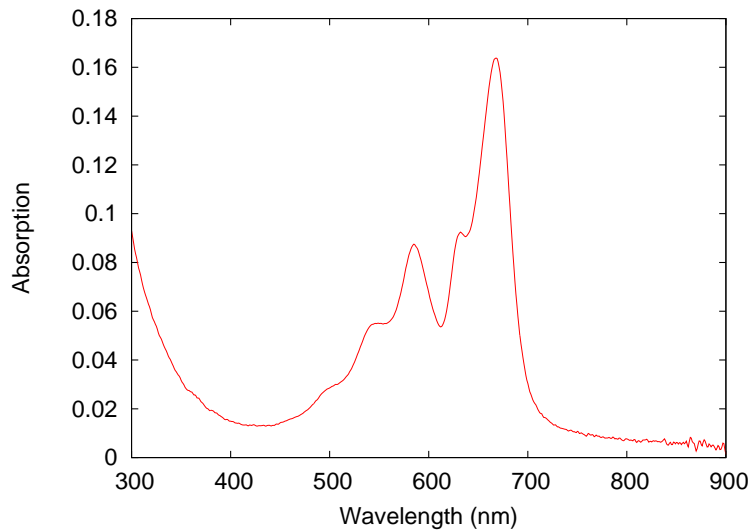


Figure 4.1: Absorption spectrum of pentacene between 300 and 900 nm

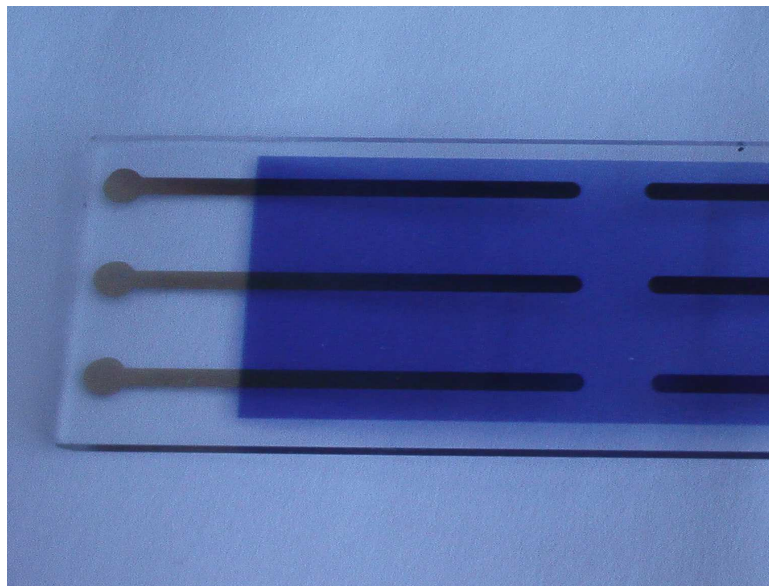


Figure 4.2: Photograph of pentacene thin film on glass slide (75.6mm \times 25.4mm)

4.2 Conductivity

4.2.1 Glass conductivity

Currents at voltages varying between +50 V and -50 V (in steps of 1 V) were measured across a number of contacts (section 3.3). Figure 4.3 shows a graph of current versus voltage for various contacts, with figure 4.4 showing the best-fit lines, obtained using linear regression (the program used is in appendix A). That the graph is linear indicates that glass is an Ohmic conductor (with a high resistance).

If a plot of resistance against number of contacts (i.e. distance across the glass is plotted), then the graph shown in figure 4.5 is obtained. Although it is expected to be a straight line, the fact that it is not indicates some error – this is quite likely due to contact resistance between the metal and the glass being significant compared to the resistance of the glass itself.

The resistance of the glass between two adjacent contacts was $1.3 \times 10^{11} \Omega$. The resistivity can be obtained using $\rho = \frac{RA}{L}$, where A is the cross-sectional area of the glass slide between the contacts, and L is the length between contacts. Given that the length of the slide is 75.5 mm, and the height is 1.0 mm (giving a cross-sectional area of 75.5 mm²), and the distance between contacts is 1.4 mm, then, assuming a uniform current density throughout the glass, this gives a resistivity value of $7 \times 10^{11} \Omega \text{ cm}$, which is within the range usually quoted for glass ($10^8 - 10^{12} \Omega \text{ cm}$).

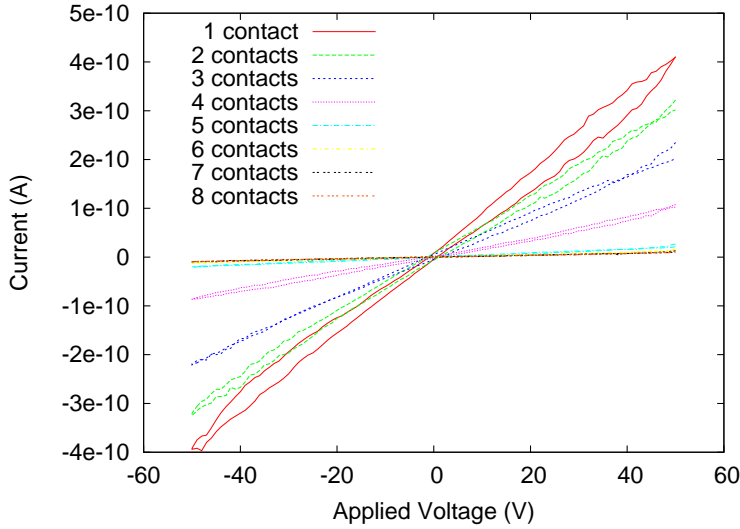


Figure 4.3: Current vs. voltage for various contacts for Chrome/Gold on glass

4.2.2 Pentacene conductivity

The pentacene conductivity experiments were carried out in a number of environments — darkness, ambient lab light, under a 60 W incandescent bulb, in a nitrogen atmosphere in the dark, and in a 2-bar nitrogen atmosphere in the dark. Figure 4.6 indicates the resistance of pentacene in the various environments between a pair of adjacent contacts.

As can be easily seen from the graph, the charge carriers in pentacene are significantly increased in the presence of light. This is expected from the absorption spectrum, which has an absorption peak at around 680 nm; this corresponds to an energy of around 1.8 eV, the bandgap of pentacene (1.82 eV [9]).

Using linear regression techniques, the resistance of pentacene between the adjacent contacts in darkness is $1.12 \times 10^{11} \Omega$, whereas in light conditions it is $2.75 \times 10^{10} \Omega$, an increase in conductivity by a factor of 4.

Using the same values for slide length and distance between contacts, 90 nm as the thickness of the pentacene layer, and assuming that current density is uniform throughout the pentacene and no current goes through the glass, the resistivity of pentacene in the dark comes out at $5.43 \times 10^7 \Omega \text{ cm}$ (conductivity of $1.84 \times 10^{-8} \Omega^{-1} \text{ cm}^{-1}$), and pentacene in light conditions comes out as $1.33 \times 10^7 \Omega \text{ cm}$ (conductivity of $7.49 \times 10^{-8} \Omega^{-1} \text{ cm}^{-1}$). This agrees fairly well, given the assumptions made, with the findings of Minakata *et al.* [14], who reported a conductivity of $< 10^{-8} \Omega^{-1} \text{ cm}^{-1}$ for undoped pentacene films.

4.3 Transistors

Characteristic curves of the first working transistor (on $0.1 \Omega \text{ cm}$ resistivity silicon) are shown in figure 4.7. If the square root of saturation current is then plotted against gate voltage, figure 4.8 is obtained; using equation 2.2, the mobility of the charge carriers in this device is $6.3 \times 10^{-3} \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. This is

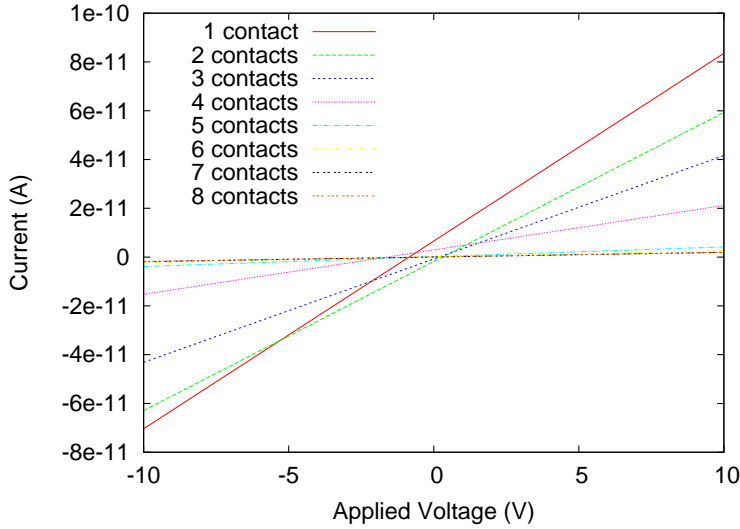


Figure 4.4: Best-fit current vs. voltage for Chrome/Gold contacts on glass

with a channel length of $70 \mu\text{m}$, channel width of 1.6 mm , SiO_2 thickness of 105 nm , taking ϵ_{OX} for SiO_2 to be 3.9 and $\epsilon_0 = 8.85 \times 10^{-14} \text{ F cm}^{-1}$.

4.3.1 DMDS surface treatments

One of the ways of improving transistor mobilities is to modify the dielectric surface; this causes the electronic properties (e.g. surface states) of the semiconductor/dielectric interface to be altered. This was done by placing one of the silicon wafers (with oxide) into a DMDS solution until a hydrophobic layer was formed; another (identical) wafer was not treated, and transistors were fabricated onto both wafers at the same time. The results of source-drain voltage/current measurements (at constant gate voltages) are shown in figure 4.10. It can be seen that with the DMDS-treated wafer saturation currents are noticeably higher (around 60% more in this case) compared with the untreated wafer. These saturation currents lead to a mobility of $3.3 \times 10^{-3} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the DMDS-treated wafer, and $1.8 \times 10^{-3} \text{ cm}^2 \text{V}^{-1} \text{s}^{-1}$ for the untreated wafer — i.e. the DMDS treatment increased the mobility by approximately 80%.

4.3.2 A higher mobility transistor

A higher mobility transistor was later fabricated on a highly conducting (approximately $10^{-3} \Omega \text{ cm}$ resistivity) silicon wafer, using around 120 nm SiO_2 treated in DMDS. Around 25 nm of pentacene was evaporated at a pressure of $1.7 \times 10^{-4} \text{ mbar}$; the wafer was then placed into an oven at $120 \text{ }^\circ\text{C}$ for 30 minutes* before 30 nm gold contacts were evaporated onto the pentacene, with a channel length of $50 \mu\text{m}$. The source-drain characteristics are shown

*This was done in order to see if the pentacene grains would rearrange themselves in a way that could improve conductivity. Unfortunately the transistors on the wafer that was not placed in the oven did not show any field effect, so no comparison can be made

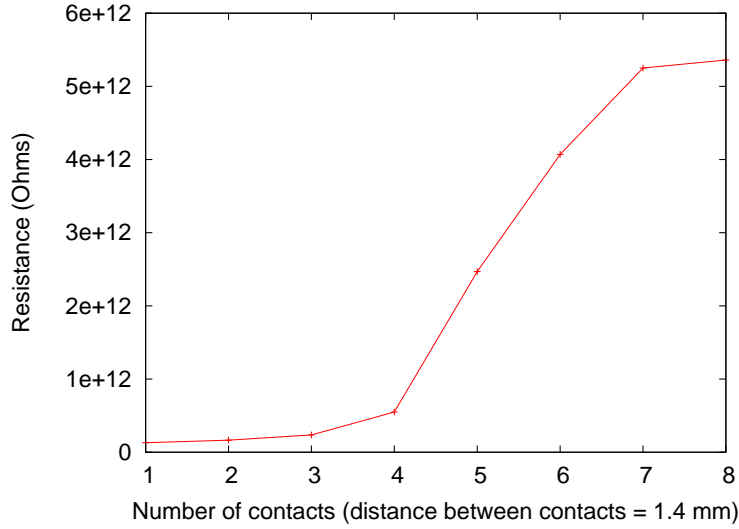


Figure 4.5: Resistance vs. distance for contacts on glass slide

in figure 4.9; it can be seen that the saturation currents are an order of magnitude larger than the ones shown in figure 4.10, which were measured using less-conducting silicon (around $0.1 \Omega \text{ cm}$ resistivity). This is reflected in the mobility, $0.032 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$, which is almost 10 times greater than the mobility obtained in the DMDS-treated wafer, reported in section 4.3.1.

A plot of current against gate voltage for this transistor is shown in figure 4.11. If we look at the Levinson plot (section 2.2.2) of $\ln(I_D/V_G)$ against $1/V_G$ for the linear region of this figure 4.11, then figure 4.12 is obtained (with a best-fit line). The slope of the plot comes out as -17.8. Using equation 2.5, and taking the semiconductor thickness as 25 nm and room temperature to be 294 K, this gives the trap density, N_t as $2.544 \times 10^{18} \text{ cm}^{-2}$. Using equation 2.4, at a gate voltage of -50 V, this gives the potential barrier height, E_B , to be 9 meV, and the trap-free mobility, μ_0 , to be $0.045 \text{ cm}^2 \text{ V}^{-1} \text{ s}^{-1}$.

4.3.3 Alternative gates

Unfortunately all the transistors made using alternate gate fabrication methods (section 3.4.1) exhibited no field effect and hence no results are shown. This may be due to some overlap between the gate metal and the semiconductor or due to bad contact between the gate metal and the silicon wafer.

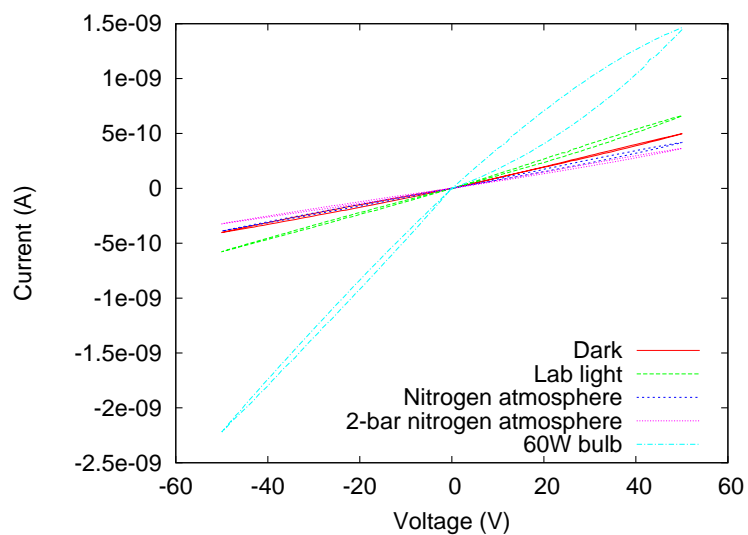


Figure 4.6: Voltage/current characteristics of adjacent contacts on pentacene in various atmospheres

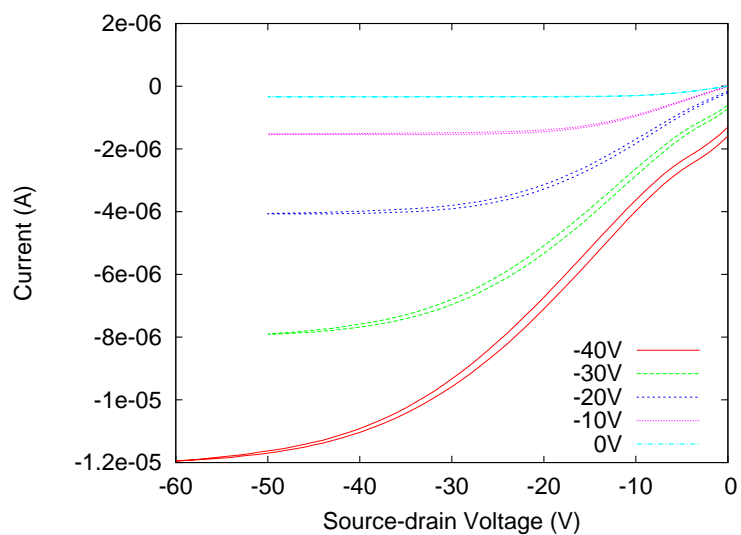


Figure 4.7: Source-drain currents against applied source-drain voltages at constant gate voltages

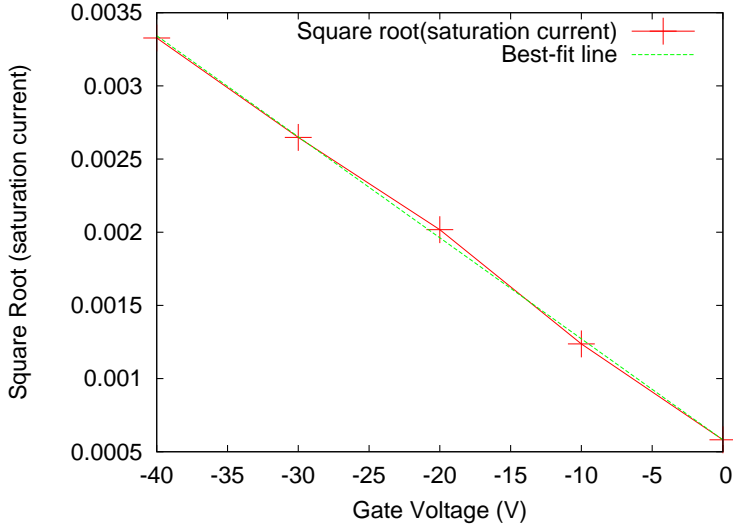


Figure 4.8: Square root of saturation current against gate voltage

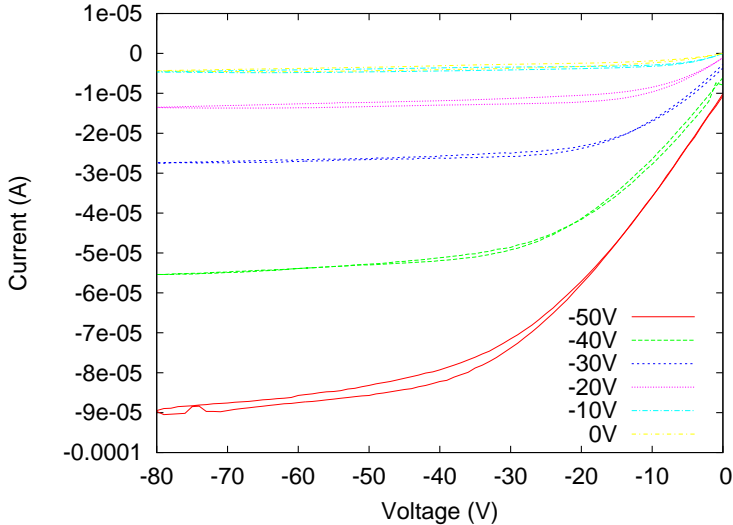
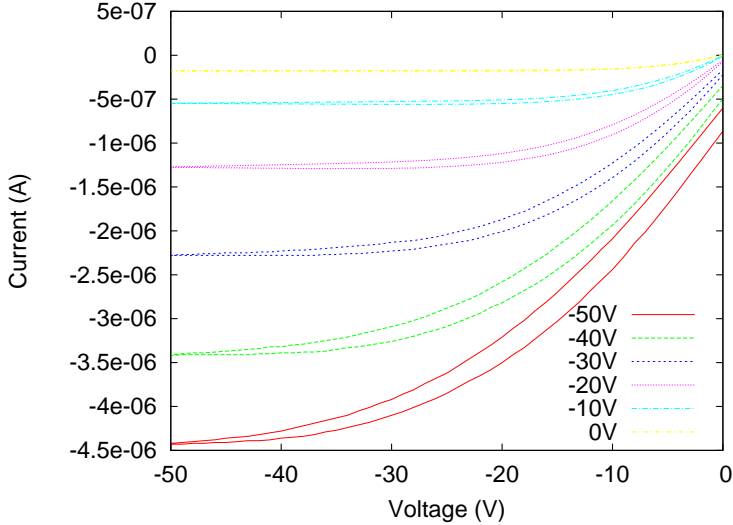
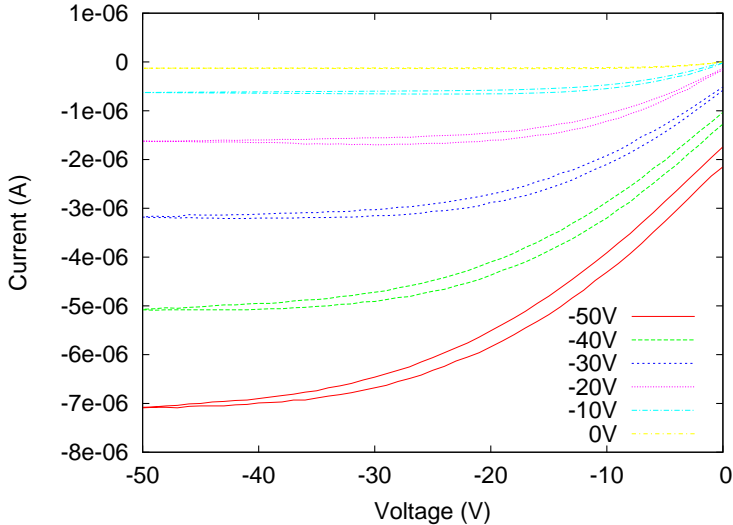


Figure 4.9: Source-drain current vs. voltage characteristics at constant gate voltage



(a) Non-DMDS treated



(b) DMDS treated

Figure 4.10: Source-drain currents against applied source-drain voltages at constant gate voltages

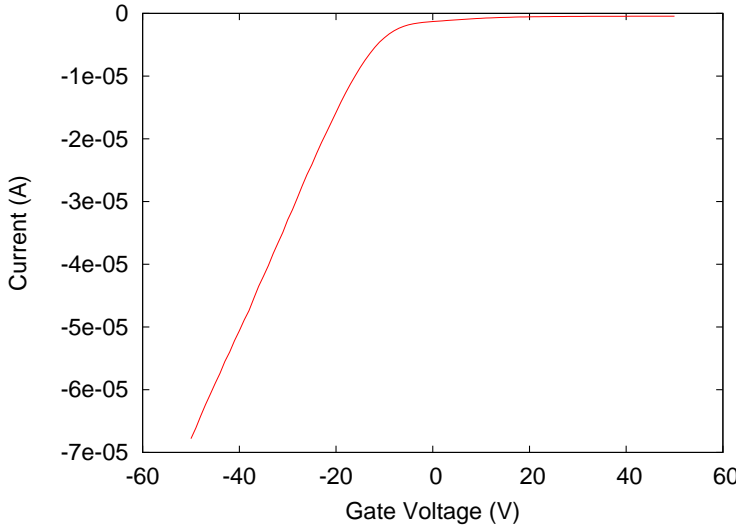


Figure 4.11: Source-drain current vs. gate voltage at constant source-drain voltage (-20V)

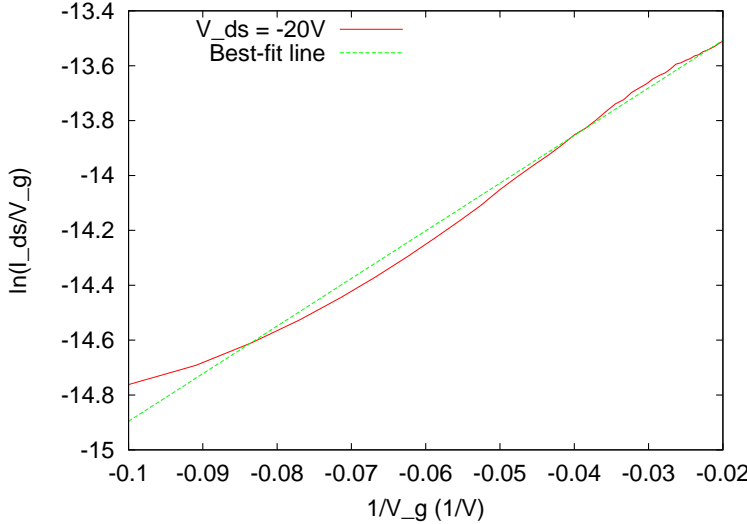


Figure 4.12: Levinson plot for the linear region of the transistor with a source-drain voltage of -20V

Chapter 5

Conclusions and Further Work

5.1 Conclusions

An absorption spectrum of pentacene was obtained, which gave a result comparable to one in published literature [12]. Conductivity measurements on pentacene in various environments, and a comparison with glass conductivity were made, with good results. A number of transistors were made; ones that did not exhibit field effects were not presented in the report. The mobility of the transistor reported in section 4.3.2 is comparable to one fabricated by Daraktchiev *et al.* [3], which uses a very similar fabrication method; their mobility was $0.1 \text{ cm}^2\text{V}^{-1}\text{s}^{-1}$, around 3 times higher than the one reported in this paper.

5.2 Further Work

There are many ways of extending this work into transistors. One possibility is to use different substrates, such as ITO-coated glass, or a flexible substrate. Another is to use a different dielectric material (e.g. PMMA or aluminium oxide). To attempt to improve mobilities and/or reduce leakage currents, a layer of nanoparticles can be laid down onto the dielectric layer.

An investigation can be carried out into patterning the gate so as to isolate individual transistors and connect them to form useful circuits; this may also involve investigation into the best way of isolating the transistors to minimise leakage between them.

Creating flash memories can also be investigated; this would be continuing previous work done in Durham in collaboration with the National Technical University of Athens [15, 8].

Lastly, different semiconducting materials may be investigated. At the time of writing this report, some initial investigation had begun into a new chemical synthesised at the Department of Chemistry, known as IR-35F (structure shown in figure 5.1), which is thought to be an *n*-type organic semiconductor. However, all data that has so far been obtained about it is an absorption spectrum, which is shown in figure 5.2.

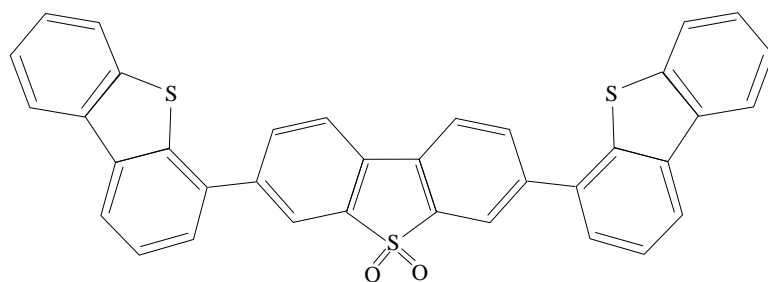


Figure 5.1: The IR-35F molecule

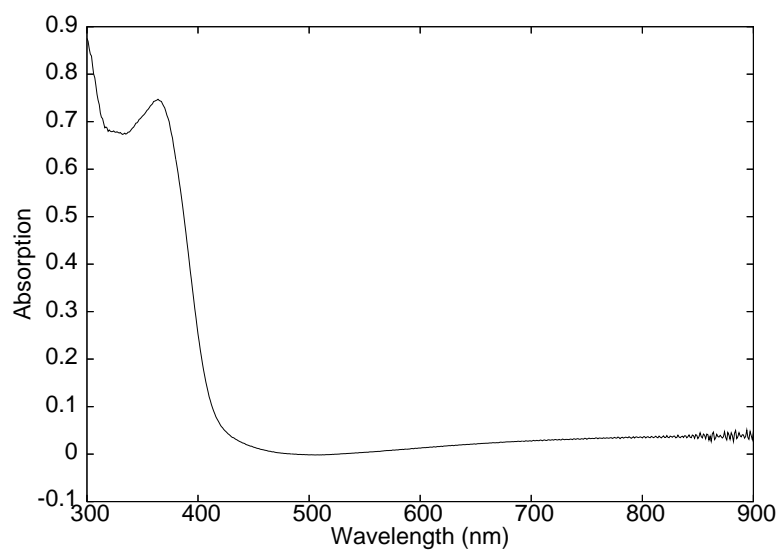


Figure 5.2: Absorption spectrum of IR-35F

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Appendix A

Regression program

```
#include<stdio.h>
#include<math.h>
#include<stdlib.h>

int main(int argc, char *argv[]) {
    FILE *file;
    int volt;
    char *foo;
    double a,b,current;
    int Sx=0;
    double Sy=0.0;
    int Sxx=0;
    double Sxy=0.0;
    int n=0;

    foo=malloc(40);

    if (argc!=2) {
        fprintf(stderr,"Wrong no. of arguments");
        return(1);
    }

    /* Open the file for reading */
    file = fopen(argv[1],"r");
    if (!file) {
        fprintf(stderr,"Unable to open file");
        return(1);
    }

    fscanf(file,"%i %s",&volt,foo);
    while (!feof(file)) {
        current=strtod(foo,NULL);
        Sx += volt;
        Sy += current;
        Sxx += (volt * volt);
    }
}
```

```
        Sxy += volt * current;
        n++;
        fscanf(file,"%i %s",&volt,foo);
    }
    fclose(file);

    b = (n*Sxy - Sx*Sy) / (n*Sxx - Sx*Sx);
    a = (Sy - b*Sx)/n;

    fprintf(stdout,"For y = a + bx, a = %e, b = %e; Resistance: %e Ohms",a,b,1/b);

    return(0);
}
```